dress. There is a carefully defined protocol that provides for acknowledgement of write transactions and returning data for read transactions. In a multimaster configuration, collision detection can be implemented along with an appropriate access arbitration algorithm.

I^2C is implemented using only two wires, but this apparent simplicity belies its flexibility. The protocol is rich in handling special situations such as multiple masters, slow slaves that cannot respond to requests at the master's SCL frequency, and error acknowledgements. Some manufacturers that incorporate I^2C into their products pay Philips a licensing fee and are therefore able to use the trademark name in their documentation. Other manufacturers try to save some money by designing what is clearly an I^2C interface but referring to it by some generic or proprietary name such as "standard two-wire serial interface." If you come across such a product, spend a few minutes reading its documentation to make sure whether a true I^2C interface is supported.

Motorola's SPI consists of a clock signal, SCK, two unidirectional data signals, and multiple slave select signals, SS* as shown in Fig. 5.20. One data signal runs from the master to each slave and is called MOSI: master-out, slave-in. The other data signal is shared by the slaves to send data back to the master and is called MISO: master-in, slave-out. SCK is always driven by the master and can be up to several megahertz. Rather than assigning a unique address to each slave, the master must assert a unique SS* to the particular device with which it wants to exchange data. On observing SS* being asserted, a slave loads the bits on the MOSI signal into an internal shift register. If a read is being performed, the slave can reply with data shifted out onto the MISO signal. Because MISO is shared by multiple slaves, they must implement some type of contention-avoidance mechanism such as tri-state or open-collector outputs.

Each of these interchip buses proves extremely useful in simplifying many system designs. It is beyond the scope of this discussion to explain the detailed workings of either I^2C or SPI. For more information, consult the technical resources available from Philips and Motorola on their web sites or in their printed data sheets.

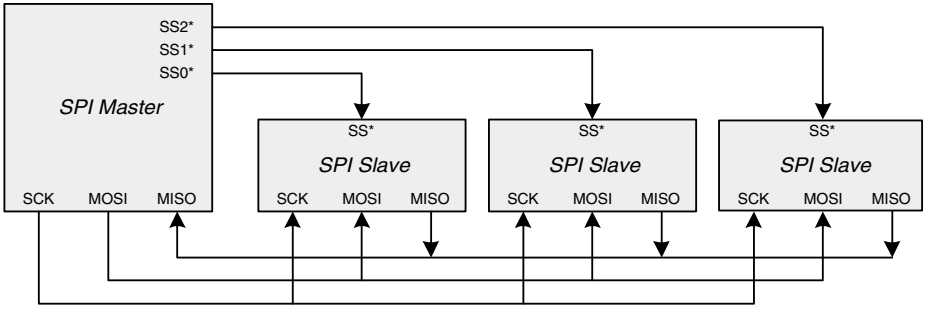

FIGURE 5.20 SPI bus organization.

CHAPTER 6
Instructive Microprocessors and Microcomputer Elements

Microprocessors, the heart of digital computers, have been in a constant state of evolution since Intel developed the first general-purpose microprocessors in the early 1970s. Intel's four-bit 4004 made history, because it was a complete microprocessor on a single chip at a time when processor modules for minicomputers filled multiple circuit boards. Over the past three decades, the complexity and throughput of microprocessors has increased dramatically as semiconductor technology has improved by leaps and bounds. Hundreds of microprocessors have come and gone over the years. There are many different architectures on the market today, each with its own claims of superior performance, lower cost, and reduced power in its intended applications.

When looking back on three decades' worth of development and the state of microprocessors today, several microprocessor families are especially worth exploring as instructional examples of basic computer architecture. Some of these families are the ancestors of very popular and widespread designs that are used to this day. Familiarity with these classic microprocessors can make it easier to learn about contemporary products that are either improved versions of the originals or members of other families that share common traits. Alternatively, some of these families are worthy of note because of their important role in permeating everyday life with microprocessors in places that most people rarely think of as computerized: cars, microwave ovens, dishwashers, and VCRs.

This chapter provides information that is both historical and directly relevant to contemporary digital systems design. Five classic microprocessor architectures are presented: Motorola 6800, Intel 8051, Microchip PIC, Intel 8086, and Motorola 68000. All of these architectures are in use today in varying forms, and each represents a different perspective on how microprocessors can accomplish similar tasks. A future design challenge may be addressed directly by one of these devices, or the solution may employ architectural concepts that they have helped to bring about.

6.1 EVOLUTION

Following the 4004's introduction in 1971, Intel enhanced the four-bit architecture by releasing the 4040 and 8008 in rapid succession. The 4040 added several instructions and internal registers, and the 8008 extended the basic architecture to eight bits. These processors ran at speeds from 100 to 200 kHz and were packaged in 16 (4004/4040) and 18 (8008) pin DIPs. While significant for their time, they had limited throughput and could address only 4 kB (4004/4040) or 16 kB (8008) of memory. In 1974, Intel made substantial improvements in microprocessor design and released the 8080, setting the stage for modern microprocessors. Whereas Intel's earlier microprocessors look like relics of a bygone era, the 8080 is architecturally not far off from many microprocessors that ex-